

CLAIMS

What is claimed is:

1. A memory device, comprising:
 - a plurality of device circuitry coupled to a plurality of device pads;
 - an operation interface to operate the memory device in an operation mode;
 - a plurality of interfaces to operate the memory device in a plurality of other modes, each interface of the plurality of interfaces having a predetermined correlation between the plurality of device circuitry and the plurality of device pads; and
 - a configuration circuit to select among the operation interface and the plurality of interfaces.
2. The memory device of claim 1, wherein the operation interface has a third set of address pads and wherein the plurality of interfaces comprises:
 - a test interface to test the memory device for defects, the test interface having a first set of address pads; and
 - a programming interface to program the memory device with a code, the programming interface having a second set of address pads.
3. The memory device of claim 2, wherein the first set of address pads enables parallel addressing of the memory device in one cycle.

1 4. The memory device of claim 3, wherein the test interface is a
2 standard flash memory interface.

1 5. The memory device of claim 2, wherein the second set of address
2 pads of the programming interface has fewer address pads than the first
3 set of address pads of the test interface.

1 6. The memory device of claim 2, wherein the third set of address
2 pads of the operation interface are multiplexed address and data pads.

1 7. The memory device of claim 6, wherein the operation interface
2 is a proprietary interface.

1 8. The memory device of claim 1, wherein the configuration circuit
2 comprises:

3 a plurality of drivers, each of the plurality of drivers coupled
4 between a device pad and a device circuit, each of the plurality of
5 drivers having a control input; and

6 a multiplexer coupled to the control input of each of the
7 plurality of drivers to select one of the plurality of drivers.

1 9. The memory device of claim 8, wherein the operation interface
2 has a third set of address pads and wherein the plurality of interfaces
3 comprises:

4 a test interface to test the memory device for defects, the test
5 interface having a first set of address pads; and

6 a programming interface to program the memory device with a
7 code, the programming interface having a second set of address pads.

1 10. A component board, comprising:

2 a processor; and

3 a memory coupled to the processor, the memory comprising:

4 a plurality of device circuitry coupled to a plurality of
5 device pads;

6 an operation interface to operate the memory in an
7 operation mode;

8 a plurality of interfaces to operate the memory in a
9 plurality of other modes, each interface of the plurality of
10 interfaces having a predetermined correlation between the
11 plurality of device circuitry and the plurality of device pads; and

12 a configuration circuit to select among the operation
13 interface and the plurality of interfaces.

1 11. The component board of claim 10, wherein the configuration
2 circuit comprises:

3 a plurality of drivers, each of the plurality of drivers coupled
4 between a device pad and a device circuit, each of the plurality of
5 drivers having a control input; and

6 a multiplexer coupled to the control input of each of the
7 plurality of drivers to select one of the plurality of drivers.

1 12. The component board of claim 11, wherein the plurality of
2 interfaces comprises:

3 a test interface to test the memory; and
4 a programming interface to program the memory with a code.

1 13. The component board of claim 12, wherein the BIOS memory is
2 a flash memory.

1 14. The component board of claim 13, wherein the test interface is a
2 standard flash interface and wherein the operation interface is a
3 proprietary interface.

1 15. A computer system, comprising:

2 a peripheral device; and

3 a system board coupled to the peripheral device, the system
4 board comprising:

5 a processor; and

6 a memory coupled to the processor, the memory

7 comprising:

8 a plurality of device circuitry coupled to a plurality
9 of device pads;

10 an operation interface to operate the memory in the
11 computer system;

12 a plurality of interfaces to operate the memory in a
13 plurality of modes, each interface of the plurality of
14 interfaces having a predetermined correlation between
15 the plurality of device circuitry and the plurality of device
16 pads; and

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a configuration circuit to select among the
operation interface and the plurality of interfaces.

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16. The computer system of claim 15, wherein the plurality of
interfaces comprises:

a test interface to test the memory; and

a programming interface to program the memory.

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17. The computer system of claim 16, wherein the BIOS memory is a
flash memory.

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18. The computer system of claim 17, wherein the test interface is a
standard flash interface and wherein the operation interface is a
proprietary interface.

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